Architecture Architecture/Computer Organization

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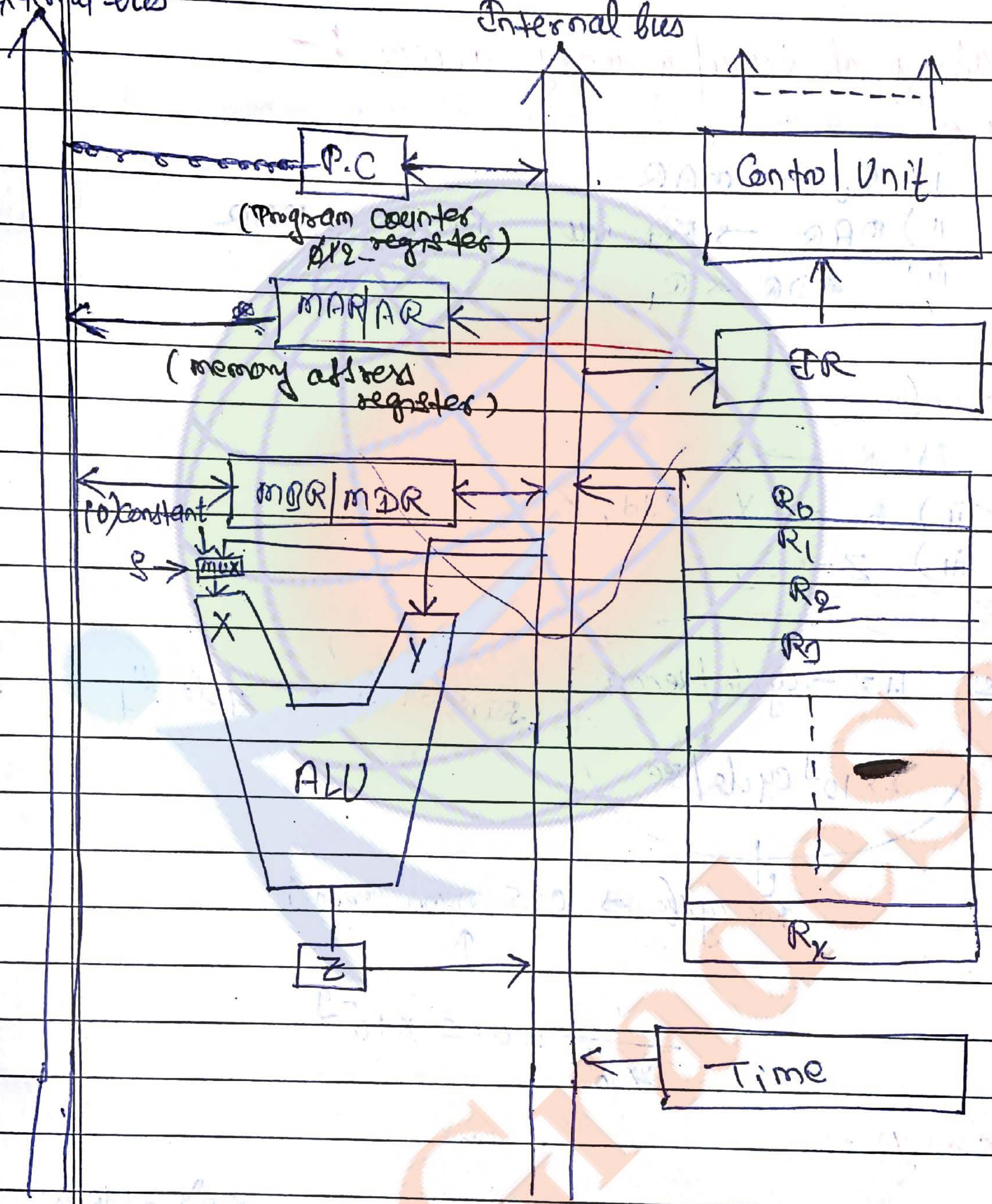
2.) CPU design! (External) मी बाहर से दिख रहा है

Internal organization

2.2 Data Path:- (Internal organisation of the Proces)



Steps!

1) Instruction fetch!-

Step - i) $PC_0 \rightarrow MAR$

Step - ii) $PC \rightarrow Y$, $MAR \rightarrow$ External bus

External bus $\rightarrow$ MDR

Step - iii) $MDR \rightarrow IR$, $Z \rightarrow PC$

a + b = c

decode

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2.) Instruction decoding:- Instruction is divided/decoded into micro instruction in specific sequence

3.) Loading of data/memory access :-
phase:

i) $R_0 \rightarrow MAR$

ii) $MAR \rightarrow$ Ext. Bus , Ext. Bus $\rightarrow MDR$

iii) $MDR \rightarrow R_1$

4.) Execution :-

i) $R_1 \rightarrow X$

v.v.I ii) $R_2 \rightarrow Y$, Add, Z

iii) $Z \rightarrow R_3$

This is cycle of CPU

Note: 1 Hz → cycle/second

2×10^9 cycle/sec

इसमें से मै तीन cycle लूँगा।

One cycle ⇒ 0.5 nano seconds

$$\frac{1}{2 \times 10^9} = 0.5 \times 10^{-9}$$

5.) Storing :-

i) $R_4 \rightarrow MAD$ - इससे address जाएगा।

ii) $R_3 \rightarrow MDR$ - इससे data जाएगा

iii) store external

3.1 Performance of CPU / Processor :-

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Performance is the indirect measurement. so it is measures by two factors:

a) execution time &
b) through put

a) Execution time :- Execution time is inversly proportional to performance

$$P \propto \frac{1}{ET}$$

execution time is suitable for the performance of uniprocessor.

whereas

throughput is suitable for server and web sections

b) Throughput : Throughput is directly proportional to performance

$$P \propto T_P$$

3.2 # Speed up :-

$$\text{Speed up} = \frac{\text{Performee of new system}}{\text{Performance of old system}}$$

But in respect/according to execution time :-

$$S = \frac{\text{Perfor. of new system}}{\text{Performance of old sys}} = \frac{\frac{1}{ET_{new}}}{\frac{1}{ET_{old}}} = \frac{ET_{old}}{ET_{new}}$$

$$= \frac{TP_{new}}{TP_{old}}$$

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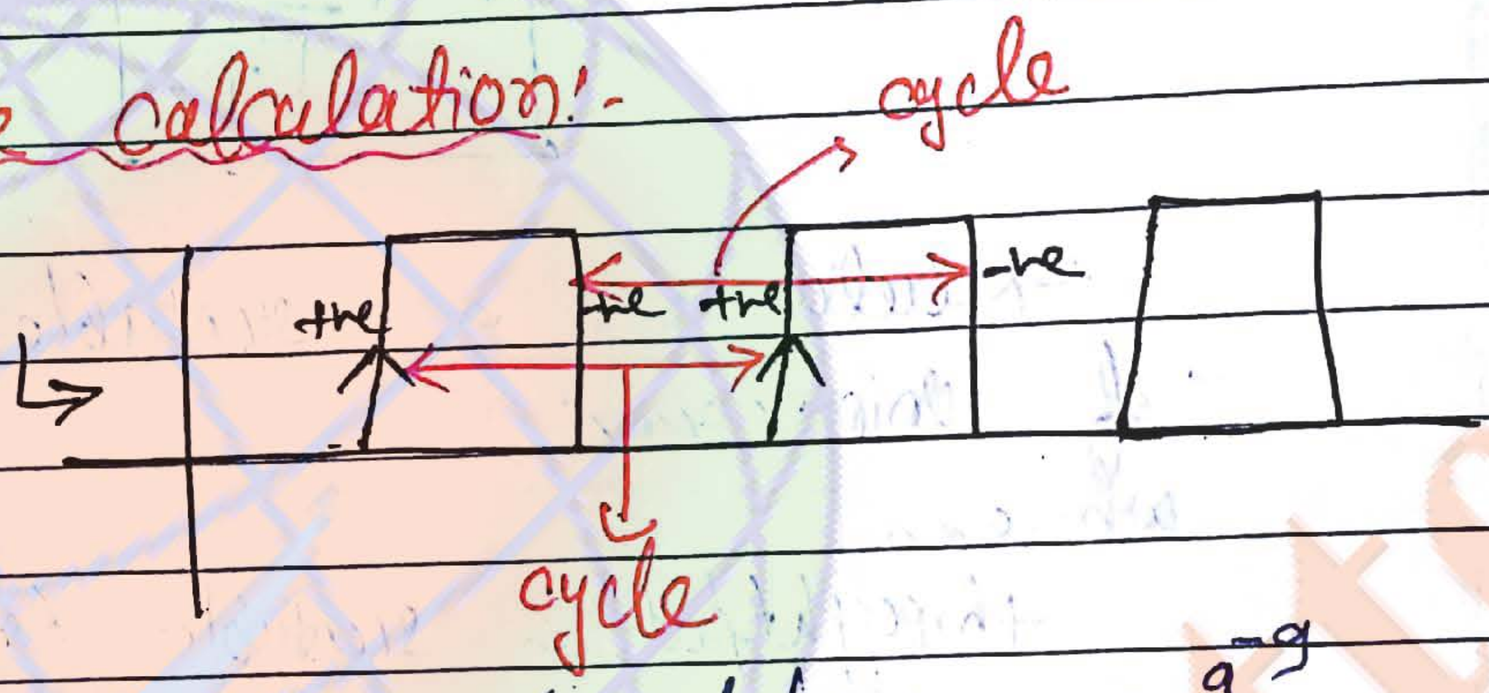
speed up factor is uses to check the performance gain of new system and old system.

$S = N \Rightarrow$ means new system will run n-time faster than old system.

- CPU time calculation:-



1 GHZ $= 1 \times 10^9$ cycle/sec $= 10^{-9}$

2 GHZ $= 2 \times 10^9$ " $= 0.5 \times 10^{-9}$

3 GHZ $= 3 \times 3^9$ " $= 0.25 \times 10^{-9}$ for one cycle time

CPU time is calculated based on two factors

i) cycle
ii) cycle time

i) cycle:- cycle is defines as clock pulse transition either from the edge to the edge or from -ve edge to -ve edge.

ii) cycle time
Amount of the time required to transfer the clock pulse either from the edge to the edge or -ve edge to -ve edge is known as cycle time.
cycle time depend on frequency of processor clock

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cycle time $\propto \frac{1}{\text{frequency of clock}}$

CPU time = No. of Instruction

CPU time = Instruction count (IC) × Clock per instruction (CPI) × one cycle time

Q) Consider 3.2 GHz processor use to execute the following segment Program contain different type of instruction.

Instruction time	Instruction count	CPI (clock per instruction)
Load	200	12
store	300	10
Arithmetic	200	8
logical	100	6
shift	150	4
branch	50	2

a) what is the avg. instruction execution time

b) what is the MIPS rate

c) what is the program execution time

Sol'n a) $\text{cycles} = \frac{200\times12 + 300\times10 + 200\times8 + 100\times6 + 150\times4 + 50\times2}{200 + 300 + 200 + 100 + 150 + 50}$

$= \frac{2400 + 3000 + 1600 + 600 + 600 + 100}{1000} = \frac{8300}{1000} = 8.3$ cycle/instruction